REMARKS

By this Amendment, claims 1, 9 and 14 are amended, and claim 7 is cancelled. Claims 5-6, 8, 10-13 and 15-21 remain in the application. Thus, claims 1, 5-6 and 8-21 are active in the application. Reexamination and reconsideration of the application are respectfully requested.

On page 2 of the Office Action, claim 9 was objected to because of the identified informalities. In particular, the Examiner noted that the term "writing pattern" in line 9 of claim 9 appeared to be a typographical error. Further, the Examiner noted that even if the term "writing pattern" was intended to mean "wiring pattern," the limitation "said wiring pattern" lacked proper antecedent basis.

Claim 9 has been amended to recite that an insulating film is formed on "said conductive pattern and said plurality of dummy patterns." Line 3 of claim 9 recites that the semiconductor device comprises "a conductive pattern formed on said pattern area of said semiconductor substrate." Accordingly, the Applicant respectfully submits that the limitation "said conductive pattern" in line 9 of claim 9 has proper antecedent basis and overcomes the objection to claim 9.

Therefore, the Applicant respectfully requests that the objection to claim 9 be withdrawn.

On page 2 of the Office Action, claims 1 and 5-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Takizawa (U.S. 6,504,254).

Without intending to acquiesce to this rejection, independent claims 1, 9 and 14 have each been amended to more clearly illustrate the marked differences between the present invention and the applied reference. Accordingly, the Applicant respectfully submits that the present invention is patentable over the applied reference for the following reasons.

The present invention provides a semiconductor device having a plurality of characteristic dummy patterns. The dummy patterns are formed in a pattern non-forming region or a non-pattern area within a same shape or having a same outline, as shown in Figures 1(A), 3(A), 4(A) and 5(A). In each shape or outline, a plurality of dummy line patterns (Figure 1(A)) or a single pattern with an opening (Figures 3(A), 4(A) and 5(A)) are formed.

As described in line 11 on page 2 to line 2 on page 3 of the substitute specification (line 13 on page 2 to line 5 on page 3 of the original specification), an insertion of dummy patterns reduces the global step so that a chemical mechanical polishing (CMP) of the insulating layer is thereby improved. However, an insertion of dummy patterns makes a pattern ratio large. Therefore, a disadvantage occurs with regard to an end detection of etching the pattern.

However, since each shape or outline of the dummy patterns of the present invention has a space portion (a space between the line patterns or the opening), a pattern ratio of the semiconductor device is reduced. Therefore, it is possible to more effectively suppress an increase in the global step that is formed by a deposition process (see, for example, lines 8-13 on page 9 of the substitute specification (lines 5-9 on page 10 of the original specification)).

For instance, Figure 1(A) of the present invention illustrates that each of the plurality of dummy patterns 14 has a plurality of line patterns 14a. Each of the line patterns 14a of each of the plurality of dummy patterns 14 is spaced from each other, and an area between each of the line patterns 14a (corresponding to a slit 14b) is filled by the deposition of an insulating film (see Figure 1(B) and Figure 2(B)). Furthermore, the present invention provides that the distance (corresponding to the slit 14b) between each of the plurality line patterns 14a is less than 72 μm (see, for example, lines 9-10 on page 8 of the substitute specification (lines 24-26 on page 8 of the original specification)).

Figure 3(A) of the present invention illustrates that each of the plurality of characteristic dummy patterns 14 has the same continuous rectangular outline shape as each other and are arranged in a matrix with predetermined spacing. Furthermore, each of the rectangular-shaped dummy patterns 14 has an opening 14c. The present invention provides that the width of the opening 14c of each the plurality dummy patterns 14 is less than 72 μm.

Furthermore, Figures 4(A) and 5(A) of the present invention illustrate that each of the plurality of characteristic dummy patterns 14 has the same shape as each other, and each of the plurality of dummy patterns 14 has a space portion 14c. The space portion 14c of each of the plurality of dummy patterns 14 indicates a shape of at least one of a

letter and graphic, and the space portion 14c of each of the plurality of dummy patterns has a width less than 72 μm.

Independent claims 1, 9 and 14 recite the semiconductor device of the present invention as having the above-described features.

In particular, claim 1 recites the semiconductor device of the present invention as comprising a plurality of dummy patterns, where each of the plurality of dummy patterns has a plurality of line patterns. Furthermore, claim 1 recites that each of the plurality of line patterns is spaced apart from each other by an area filled by the deposition of the insulating film, and that a distance between each of the plurality of line patterns is less than 72 μm.

Claim 9 recites the semiconductor device of the present invention as comprising a plurality of dummy patterns, where each of the plurality of dummy patterns has a same continuous rectangular outline shape as each other and is arranged in a matrix with predetermined spacing. Furthermore, claim 9 recites that each of the plurality of dummy patterns has an opening so that a pattern ratio of the semiconductor device is reduced, and that a width of the opening of each of the plurality of dummy patterns is less than 72 μm.

Claim 14 recites the semiconductor device of the present invention as comprising a plurality of dummy patterns being formed in a plurality of dummy areas, and that each of the plurality of dummy patterns has a space portion within each of the dummy areas so that a pattern ratio of the semiconductor device is reduced. Furthermore, claim 14 recites that each space portion of the plurality of dummy patterns indicates a shape of at least one of a letter and graphic, and that each space portion of the plurality of dummy patterns has a width less than 72 μm.

Takizawa merely discloses hexagonal-shaped dummy patterns have one opening (Figure 2) or a plurality of openings (Figure 4). Thus, the dummy patterns of Takizawa are clearly different from a dummy pattern comprising a plurality of line patterns, as recited in claim 1, and a dummy pattern having a space portion to indicate a shape of at least one of a letter and a graphic, as recited in claim 14. Furthermore, Takizawa does not disclose or suggest that an opening is filled by a dielectric layer 40 to reduce a pattern ratio of the semiconductor device, as recited in claim 9.

With reference to Column 6, lines 37-38, the Examiner contends that Takizawa discloses that an area between each of the plurality of dummy patterns is less than 72 μm because the width of the dummy wiring section 30 is less than 2 μm (see also Column 2, lines 35-42).

However, as described above, claim 1 recites that each of the plurality of dummy patterns has a plurality of line patterns, and that a distance between each of the plurality of line patterns is less than 72 μm.

Claim 9 recites that each space portion of the plurality of dummy patterns has a width less than 72 μm. Claim 14 recites that each space portion of the plurality of dummy patterns has a width less than 72 μm.

These limitations of claims 1, 9 and 14 are clearly not disclosed, suggested or even contemplated by Takizawa.

Accordingly, for at least the foregoing reasons, the Applicant respect submits that Takizawa clearly fails to disclose or suggest each and every limitation of claims 1, 9 and 14.

Therefore, the Applicant respectfully submits that claims 1, 9 and 14 are clearly patentable over Takizawa since Takizawa fails to disclose or suggest each and every limitation of claims 1, 9 and 14.

Furthermore, it is submitted that the clear distinctions discussed above are such that a person having ordinary skill in the art at the time the invention was made would not have been motivated to modify Takizawa in such a manner as to result in, or otherwise render obvious, the present invention as recited in claims 1, 9 and 14.

Therefore, it is submitted that the claims 1, 9 and 14, as well as claims 5-6 and 8, 10-13 and 15-21 which depend therefrom, are clearly allowable over the prior art as applied by the Examiner.

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. An early notice thereof is respectfully solicited.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

Takeshi MORITA

By: _____

Jonathan R. Bowser
Registration No. 54,574
Attorney for Applicant

JRB/nrj
Washington, D.C. 20006-1021
Telephone (202) 721-8200
Facsimile (202) 721-8250
October 3, 2006